IVB.Tech I Semester (E.C.E)

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23A04703a	**LOW POWER VLSI DESIGN**	3	0	0	3

Course Objectives:

1. To understand the need for low-power circuit design and analyze different power dissipation mechanisms in VLSI circuits.
2. To explore various low-power design approaches at the system, circuit, and mask levels.
3. To study low-power adder architectures and their role in power-efficient computing.
4. To examine different low-power multiplier architectures and their impact on digital design.
5. To gain knowledge of low-power memory technologies and their future developments.

Course Outcomes:

After completing the course, the student will be able to,

1. Understand the need for low-power circuit design and analyze different power dissipation mechanisms in VLSI circuits.
2. Learn various low-power design approaches at the system, circuit, and mask levels.
3. Gain knowledge on low-power adder architectures and their role in power-efficient computing.
4. Examine different low-power multiplier architectures and their impact on digital design.
5. Grasp knowledge of low-power memory technologies and their future developments.

UNIT I

Fundamentals: Need for Low Power Circuit Design, Sources of Power Dissipation – Static and Dynamic Power Dissipation, Short Circuit Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT II

Low-Power Design Approaches: Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches. Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT III

Low-Voltage Low-Power Adders: Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look Ahead Adders, Carry Select Adders, Carry

Save Adders, Low-Voltage Low-Power Design Techniques – Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT IV

Low-Voltage Low-Power Multipliers: Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT V

Low-Voltage Low-Power Memories: Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

Textbooks:

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

References:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC
   Press, 2011.
2. Low Power CMOS Design – AnanthaChandrakasan, IEEE Press/Wiley International, 1998.
3. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons,2000.