IVB.Tech I Semester (E.C.E)

23A04702b	**DSP PROCESSORS & ARCHITECTURES**	**L**	**T**	**P**	**C**
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Course Objectives:

1. To describe the unique features and significance of Digital Signal Processing (DSP).
2. To demonstrate various computational parameters and accuracy considerations in DSP systems.
3. To introduce architectural improvements in programmable DSP devices and their execution models.
4. To expose students to basic DSP algorithms, including filtering, FFT, and adaptive processing.
5. To outline DSP processor applications and their interfacing with memory and I/O peripherals.

Course Outcomes:

After completing the course, the student will be able to,

1. Summarize the fundamental features and role of Digital Signal Processing in real-world applications.
2. Evaluate dynamic range, precision, and error sources in DSP implementations.
3. Explain the architectural features of DSP processors and their computational efficiency.
4. Analyze the performance of DSP algorithms on programmable DSP platforms for specific applications.
5. Select and implement DSP processors for real-time applications, including memory and peripheral interfacing.

UNIT-I

Introduction to Digital Signal Processing: Introduction, a Digital signal-processing system, the sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), linear time-invariant systems, Digital filters, Decimation and interpolation, Analysis and Design tool for DSP Systems MATLAB, DSP using MATLAB.

Computational Accuracy in DSP Implementations: Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT-II

Architectures for Programmable DSP Devices: Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities,

Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

Execution Control and Pipelining: Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.

UNIT-III

Programmable Digital Signal Processors: Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On- Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

UNIT-IV

Implementations of Basic DSP Algorithms: The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing.

Implementation of FFT Algorithms: An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.

UNIT-V

Interfacing Memory and I/O Peripherals to Programmable DSP Devices: Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA). A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

TEXT BOOKS:

1. Avtar Singh and S. Srinivasan, "Digital Signal Processing Implementation", 1st Edition, Cengage Learning, 2004.
2. Lapsley et al. S. Chand and Co, "DSP Processor Fundamentals, Architectures & Features", 2000.

REFERENCES:

1. B. Venkata Ramani and M. Bhaskar, "Digital Signal Processors, Architecture, Programming and Applications", TMH, 2004.
2. Jonatham Stein, "Digital Signal Processing: A Computer Science Perspective", John Wiley, 2000.