III B.Tech II Semester (E.C.E)

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23A04603T	**VLSI DESIGN**	3	0	0	3

Course Objectives:

1. To understand the steps involved in fabrication of ICs using MOS transistor technology.
2. To learn about the VLSI design processes, Stick diagrams and Layouts.
3. To gain knowledge on the Gate Level Design concepts.
4. To learn the design of various subsystems with different VLSI Design styles.
5. To get familiar with CMOS testing techniques.

Course Outcomes:

At the end of the course, the students will be able to

1. Understand the steps involved in fabrication of ICs using MOS transistor technology.
2. Learn about the VLSI design processes, Stick diagrams and Layouts.
3. Gain knowledge on the Gate Level Design concepts.
4. Learn the design of various subsystems with different VLSI Design styles.
5. Familiar with CMOS testing techniques.

UNIT I

Introduction: Brief Introduction to IC technology MOS, PMOS, NMOS, CMOS & BiCMOS Technologies. Basic Electrical Properties of MOS and BiCMOS Circuits: I_{DS} - V_{DS} relationships, MOS transistor Threshold Voltage, figure of merit, Transconductance, Pass transistor, NMOS Inverter, Various pull ups, CMOS Inverter analysis and design, Bi-CMOS Inverters.

UNIT II

VLSI Circuit Design Processes: VLSI Design Flow, MOS Layers, Stick Diagrams, Design Rules and Layout, Lambda(λ)-based design rules for wires, contacts and Transistors, Layout Diagrams for NMOS and CMOS Inverters and Gates, Scaling of MOS circuits, Limitations of Scaling.

UNIT III

Gate level Design: Logic gates and other complex gates, Switch logic, Alternate gate circuits. Basic Circuit Concepts: Sheet Resistance Rs and its concepts to MOS, Area Capacitances calculations, Inverter Delays, Driving large Capacitive Loads, Wiring Capacitances, Fan-in and fan-out

UNIT IV

Subsystem Design: Shifters, Adders, ALUs, Multipliers, Parity generators, Comparators, Counters. VLSI Design styles: Full-custom, Standard Cells, Gate-arrays, FPGAs, CPLDs and

Design Approach for Full-custom and Semi-custom devices, parameters influencing low power design.

UNIT V

CMOS Testing: Need for testing, Design for testability - built in self-test (BIST) – testing combinational logic –testing sequential logic – practical design for test guide lines – scan design techniques.

Textbooks:

1. Essentials of VLSI Circuits and Systems, Kamran Eshraghian, EshraghianDougles, A. Pucknell, 2005, PHI.
2. Modern VLSI Design – Wayne Wolf, 3 Ed., 1997, Pearson Education.

References:

1. CMOS VLSI Design-A Circuits and Systems Perspective, Neil H.E Weste, David Harris, Ayan Banerjee, 3rd Edn, Pearson, 2009.
2. BehzadRazavi , "Design of Analog CMOS Integrated Circuits", McGraw Hill, 2003.
3. Jan M. Rabaey, "Digital Integrated Circuits", AnanthaChandrakasan and Borivoje Nikolic, Prentice-Hall of India Pvt.Ltd, 2nd edition, 2009.