

II Year B.Tech. – I Semester

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(23A04303T) DIGITAL CIRCUITS DESIGN

Course Objectives:

- Understand the properties of Boolean algebra, logic operations, and minimization of Boolean functions.
- Analyze combinational and analyze sequential logic circuits.
- Understand the concepts of FSM and compare various Programmable logic devices.
- Model combinational and sequential circuits using HDLs.

Course Outcomes: After completing the course, the student should be able to:

- Understand the properties of Boolean algebra, logic operations, concepts of FSM (L2)
- Apply techniques for minimization of Boolean functions (L3)
- Analyze combinational and Sequential logic circuits. (L4)
- Compare various Programmable logic devices. (L4)
- Design and Model combinational and sequential circuits using HDLs. (L5, L6)

UNIT I Boolean algebra, logic operations, and minimization of Boolean functions

Review of Number Systems and Codes, Representation of unsigned and signed integers, Floating Point representation of real numbers, Laws of Boolean Algebra, Theorems of Boolean Algebra, Realization of functions using logic gates, Canonical forms of Boolean Functions, Minimization of Functions using Karnaugh Maps.

UNIT II Combinational Logic Circuits

Combinational circuits, Design with basic logic gates, design procedure, adders, subtractors, 4-bit binary adder/ subtractor circuit, BCD adder, carry look- a-head adder, binary multiplier, magnitude comparator, data selectors, priority encoders, decoders, multiplexers, demultiplexers.

UNIT III Hardware Description Language

Introduction to Verilog - structural specification of logic circuits, behavioral specification of logic circuits, hierarchical Verilog Code, Verilog for combinational circuits - conditional operator, if-else statement, case statement, for loop using sequential circuits with CAD tools.

UNIT IV Sequential Logic Circuits

Basic architectural distinction between combinational and sequential circuits, Design procedure, latches, flip-flops, truth tables and excitation tables, timing and triggering consideration, conversion of flip- flops, design of counters, ripple counters, synchronous counters, ring counter, Johnson counter, registers, shift registers, universal shift register. Verilog constructs for sequential circuits, flip-flop with clear capability, using Verilog constructs for registers and counters.

UNIT V Finite State Machines and Programmable Logic Devices

Types of FSM, capabilities and limitations of FSM, state assignment, realization of FSM using flip-flops, Mealy to Moore conversion and vice-versa, reduction of state tables using

partition technique, Design of sequence detector. Types of PLD's: PROM, PAL, PLA, basic structure of CPLD and FPGA, advantages of FPGAs.

Textbooks:

1. M. Morris Mano, "Digital Design", 3rd Edition, PHI. (Unit I to IV)
2. Stephen Brown and Zvonko Vranesic, "Fundamentals of Digital Logic with Verilog Design", 3rd Edition, McGraw-Hill (Unit V)

Reference Books:

1. Charles H. Roth, Jr, "Fundamentals of Logic Design", 4th Edition, Jaico Publishers.
2. Zvi Kohavi and Niraj K. Jha, "Switching and Finite Automata Theory, 3rd Edition, Cambridge University Press, 2010.
3. Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", 2nd Edition, Prentice Hall PTR.
4. D.P. Leach, A.P. Malvino, "Digital Principles and Applications", TMH, 7th Edition.